REMARKS

These comments are responsive to the Official Action mailed on Office Action mailed on May 12, 2004. Claims 63-77 and 80-124 are currently pending. The Office Action rejected these claims 63-77 and 80-124 under 35 U.S.C. 112, first paragraph, for lack of support for several elements of the claims. These rejections are respectfully submitted to be in error and are each addressed under the appropriate heading below.

Additionally, claims 63-77 and 80-124 are rejected under 35 U.S.C. 102(e) as anticipated by various Banks patents. These rejections are also respectfully submitted to be in error and are all addressed under the first heading below.

Rejections under 35 U.S.C. 102(e)

The Office Action claims 63-77 under 35 U.S.C. 102(e) as anticipated by Banks (6,014,327); rejected claims 80-93 under 35 U.S.C. 102(e) as anticipated by Banks (6,344,998); rejected claims 94-106 under 35 U.S.C. 102(e) as anticipated by Banks (6,381,172); and rejected claims 107-124 under 35 U.S.C. 102(e) as anticipated by Banks (6,404,675). As specified in the "Cross-Reference to Related Application" section added to the beginning of the present application by Preliminary Amendment filed concurrently with the present application, and as is also shown on the filing receipt, the **present application is entitled to an effective filing date of April 13, 1989.**

U.S. patent 6,344,998 of Banks has a filing date of February 28, 2001, and claiming priority from a number of U.S. patent applications, the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is **well over a year after the effective filing date of the present application**.

Similarly, U.S. patent 6,014,327 of Banks has a filing date of May 14, 1999, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is **well over a year after the effective filing date of the present application**.

Similarly, U.S. patent 6,381,172 of Banks has a filing date of May 14, 1999, and claiming priority from a number of U.S. patent applications (in one case through a continuation in-part), the earliest of which has a filing date of February 27, 1995. Thus, this

earliest priority date is **several years after the effective filing date of the present application**.

Similarly, U.S. patent 6,404,675of Banks has a filing date of June 11, 2002, and claiming priority from a number of U.S. patent applications, the earliest of which has a filing date of February 8, 1991. Thus, this earliest priority date is **well over a year after the effective filing date of the present application**.

Consequently, it is therefore respectfully submitted that the rejection claims 63-77 and 80-124 under 35 U.S.C. 102(e) is not well founded and should be withdrawn.

Rejections under 35 U.S.C. 112, 1st ¶: Verifying and Reading Reference Parameters

The Office Action has rejected claims 63-77 and 80-124 under 35 U.S.C. 112, first paragraph, due to lack of support for the verifying reference parameters and for these parameters not being related to the reading reference parameters as described in the claims. This rejection is respectfully submitted to be in error. As these parameters are all similarly described in the various claims, reference will be made to claim 63, with the support for the other claims following in a similar manner. With respect to the support provided below, it is again noted that the present application presents a number of embodiment and the following support is based on only one example of these.

The Examiner's attention is directed to Attachment A, which accompanies the present Response and to which reference is made in the following.

In particular, the elements for which the Office Action fails to find support are listed below for the case of claim 63. The corresponding support is then provided for each of these with reference to the Figure 11c of the `344 patent (which is also Figure 15B of the present application), Figure 11e of the `344 patent, and the description of these figures at column 34, line 5, to column 26, line 65, of the `344 patent. Attention is particularly called to lines 4-65 of column 26.

More specifically, the verifying reference parameters are described in claim 63 as:

> verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation

for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

Support in the present application is given in Figure 11c of the `344 patent (which is also Figure 15B of the present application). These are the reference current $I_{REF("3")}$, $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-50, of `344, where the emphasis is added:

> ... For a four state storage, four sense amplifiers, each with its own distinct current reference levels IREF,0, IREF,1, IREF,2, and IREF,3 are attached to each decoded output of the bit line. ... .
>
> *During programming*, the four data inputs Ii (I0, I1, I2 and I3) are presented to a comparator circuit which also has presented to it the four sense amp outputs for the accessed cell. If Di match Ii, then the cell is in the correct state and no programming is required. If however all four Di do not match all four Ii, then the comparator output activates a programming control circuit. This circuit in turn controls the bit line (VPBL) and word line (VPWL) programming pulse generators. A single short programming pulse is applied to both the selected word line and the selected bit line. This is followed by a second read cycle to determine if a match between Di and Ii has been established. This sequence is repeated through multiple programming/reading pulses and is stopped only when a match is established (or earlier if no match has been established but after a preset maximum number of pulses has been reached).
>
> The result of such multistate programming algorithim is that <u>each cell is programmed into any one of the four conduction states in direct correlation with the reference conduction states I_{REF}, i.</u> ...

Thus, it can be seen that IREF,0, IREF,1, IREF,2, and IREF,3 correspond to the "at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter" of the claim.

The reading parameters are described in claim 63 as:

> reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

These are also shown in Figure 11c of the `344 patent (which is also Figure 15B of the present application). These are again the reference current $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-18, of `344, except that for the embodiment to which the present claims are drawn, **for the read process these are shifted with respect to their values as programming reference parameters** so that they are arranged as described in the claim. This is described at 26, lines 51-65, of `344, where the emphasis is added:

> ... only three sense amplifiers and three reference levels are required to sense the correct one of four stored states. For example, in FIG. 11c, I sub REF ("2") can differentiate correctly between conduction states "3" and "2", I sub REF ("1") can differentiate correctly between conduction states "2" and "1", and I sub REF ("0") can differentiate correctly between conduction states "1" and "0". *In a practical implementation of the circuit of FIG. 11e the reference levels I sub REF, i (i=0,1,2) may be somewhat shifted by a fixed amount during sensing to place them closer to the midpoint between the corresponding lower and higher conduction states of the cell being sensed.*

Consequently, it can be seen that the ***shifted*** values of IREF,0, IREF,1, and IREF,2 used during sensing correspond to the "at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter" of the claim.

The relation of the reading parameters to the states is described in claim 63 as:

> wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

This is illustrated in Figure A of the Attachment A, where the first read parameter is labeled as Read 1, the first state is labeled as State 1, and so on for the other read parameters and states. As described in the italicized portion of at the end of the portion of the specification quoted in the last paragraph, the *shifted* values of IREF,0, IREF,1, and IREF,2 are arranged with respect to the states of cell as shown in Figure C. Figure C corresponds to Figure 11c of '344 along the dotted line at V_{CG}=5.0, for example. It can be seen that Figure A and Figure C describe the same relations, with the following identifications: State 1~"0"; State 2~"1"; State 3~"2"; State 4~"3"; and Read 3~I_{REF} ("2"), sense; Read 2~I_{REF} ("1"), sense; Read 1~I_{REF} ("0"), sense.

The reading parameters are described further in claim 63 as:

> wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

This is just stating that each "reading reference parameter" is used for normal sensing of the state of a multi-state memory cell, as is described, for example, at column 24, lines 5-38, of the application and which is developed more fully over the next two and a half columns.

The relation of the reading parameters to verifying reference parameters is described in claim 63 as:

> wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

This is illustrated in Figure B of the Attachment A, where the first verify parameter is labeled as Verify 1 and so on for the other verify parameters. This is described at 26, lines 51-65, of `344, where the emphasis is added:

> In actual fact, although four reference levels and four sense amplifiers are used to program the cell into one of four distinct conduction states, only three sense amplifiers and three reference levels are required to sense the correct one of four stored states. For example, in FIG. 11c, I sub REF ("2") can differentiate correctly between conduction states "3" and "2", I sub REF ("1") can differentiate correctly between conduction states "2" and "1", and I sub REF ("0") can differentiate correctly between conduction states "1" and "0". *In a practical implementation of the circuit of FIG. 11e the reference levels I sub REF, i (i=0,1,2) may be somewhat shifted by a fixed amount during sensing to place them closer to the midpoint between the corresponding lower and higher conduction states of the cell being sensed.*

Consequently, the *shifted* values of IREF,0, IREF,1, and IREF,2 used as reading reference parameters are arranged with respect to the programming reference parameters IREF,0, IREF,1, IREF,2, and IREF,3 as shown in Figure D. (Figure D would again corresponds to Figure 11c of `344 along the dotted line at V_{CG}=5.0, for example.) It can be seen that Figure A and Figure C describe the same relations, with the following identifications: Verify 4~I_{REF} ("3"), program verify; Verify 3~I_{REF} ("2"), program verify; Verify 2~I_{REF} ("1"), program verify; Verify 1~I_{REF} ("0"), program verify and Read 3~I_{REF} ("2"), sense; Read 2~I_{REF} ("1"), sense; Read 1~I_{REF} ("0"), sense.

Concerning the comments of the Office Action in its paragraph 10, the Office Action admits that column 26, lines 51-65, of the `344 describes shifting the values of I_{REF} during sensing relative to that used for program verify. However, it then goes on to state that "There is no show or suggestion of separate verifying reference parameters and reading reference parameters". This is respectfully submitted to be in error. If the parameters have different values, they are different parameters. As described above, the present application is believed to clearly support what is actually found in the claims themselves as they are written.

Consequently, it is therefore respectfully submitted that the rejections under 35 U.S.C. 112, first paragraph, due to lack of support for the verifying reference parameters and for these parameters not being related to the reading reference parameters as described in the claims are not well founded and should be withdrawn. If the above does not address the particular concerns of the Examiner with respect to these elements, a phone call to the undersigned would be welcomed.

Rejections under 35 U.S.C. 112, 1st ¶: Parameter Generating Circuitry

Claims 94-106 are also rejected under 35 U.S.C. 112, first paragraph, as failing to provide an adequate written description for the parameter generating circuitry that is additionally included in these claims. These are shown in Figure 11e of the '344 patent as the current sources $I_{REF,0}$, $I_{REF,1}$, $I_{REF,2}$, $I_{REF,3}$ connected to the sense amps. Specific embodiments based on reference cells are shown in Figures 17A and 17B. Figure 17A shows MASTER REFERENCE CELL 1400 supplying current along line 1403 to SENSE AMPLIFIER 1410. Figure 17B shows reference cells 1431, 1433, 1435 supplying current along line 1441 to SENSE AMPLIFIER 1440. These circuits are described in detail in the section of the material included by the Preliminary Amendment filed concurrently with the present application entitled "Read Circuits and Techniques Using Reference Cells" which begins on page 9, line 19, of the Preliminary Amendment, with particular reference to page 12, line 6, to page 14, line 14.

Specifically, page 12, lines 20-28:

> .:. Co-pending patent application, Serial No. 204,175 proposes using the same sensing amplifiers and I_{REF}'s for both programming and reading. This provides good tracking between the reference levels (broken curves in figure 15B) and the programmed levels (solid curves in figure 15B).
>
> In the improved scheme of the present invention, the I_{REF}'s are themselves provided by the source-drain currents of a set of EEprom cells existing on the same chip and set aside solely for this purpose. Thus, they act as master reference cells with their I_{REF}'s used as reference levels for the reading and programming of all other EEprom cells on the same chip.

And at page 13, lines 12-14:

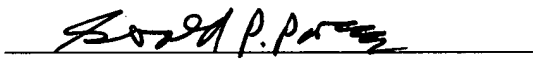
> Once the reference threshold voltage V_{TI} or reference drain-source current I_{REF} is programmed into each reference cell 1400, it then serves as a reference for the reading of an addressed memory cell such as cell 1420.

Consequently, it is therefore respectfully submitted that the rejections under 35 U.S.C. 112, first paragraph, due to lack of support for the parameter generating circuitry are not well founded and should be withdrawn.

Conclusion

Reconsideration of the rejections of claims 63-77 and 80-124 and an early indication of their allowance are solicited, and if there are any questions about the support provided above and in the previous response, a call to the undersigned is invited.

Respectfully submitted,



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Attachment A

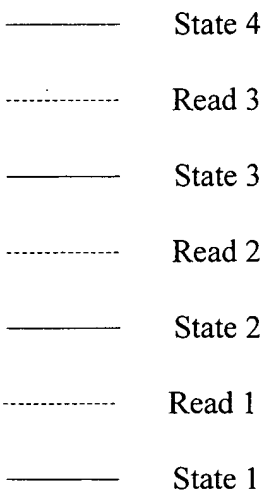

Figure A

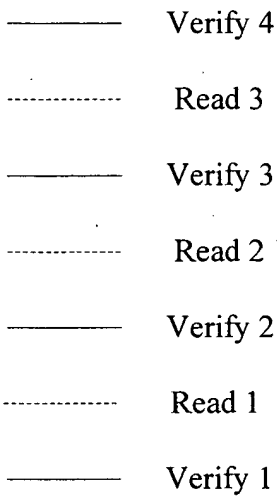

Figure B

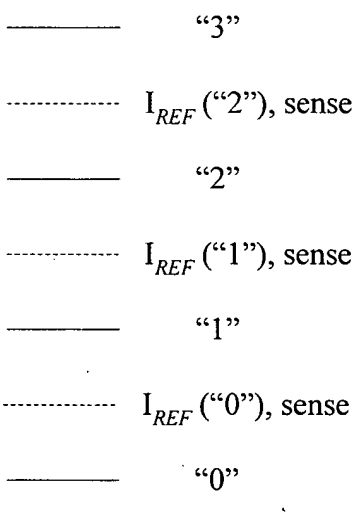

Figure C

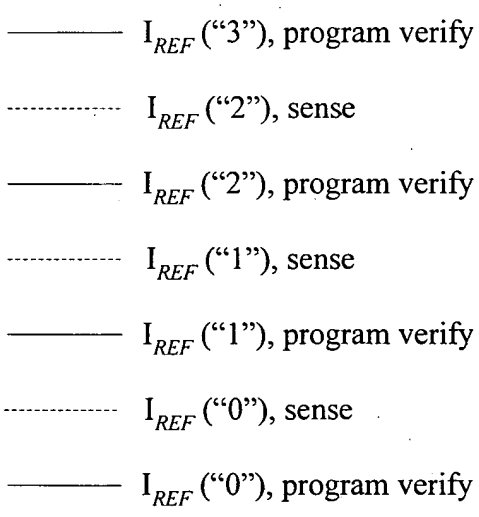

Figure D